UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,829	07/25/2001	Tsuyoshi Tamura	110196	6319

25944 7590 05/04/2005

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
NGUYEN, KEVIN M	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/911,829	TAMURA, TSUYOSHI	
	Examiner	Art Unit	
	Kevin M. Nguyen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March/30/2005 has been entered. An action on the RCE follows:

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-26 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Applicant 09/911,409.

Current application recites "a first port, a second port, a still image, a moving image, an external MPU, a RAM, a first control circuit, and a second control circuit, and

a reception circuit", whereas the conflicting current application 09/911,409 recites terms "a first bus line, a second bus line, a still image, a moving image, an external MPU, a first control circuit, and a second control circuit". It would have been obvious to make the claimed limitations of the application "a first port, a second port" and "a first bus line, a second bus line" of application 09/911,409 are different, but these limitations have the same meaning for input and/or output data.

Current application recites "a reception circuit", whereas the conflicting current application 09/911,409 does not recite "a reception circuit". It would have been obvious to make the claimed limitations of the application "a reception circuit" are narrower than the claimed limitation of application 09/911,409.

4. Claims 27, 29 and 31 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 20 of copending Applicant 09/911,409. Current application recites "the still-image data can be rewritten irrespective of the timing at which the moving-image data is rewritten in RAM", whereas the conflicting current application 09/911,409 recites "the still-image data can be rewritten irrespective of the timing at which the moving-image data is rewritten in RAM" and does not recite "a reception circuit". It would have been obvious to make the claimed limitations of the application "a reception circuit" are narrower than the claimed limitation of application 09/911,409.

5. Claims 28, 30 and 32 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 21 of copending Applicant 09/911,409. Current application recites "a first control circuit which

controls writing or reading of the still-image data and (emphasis) the moving-image data...", whereas the conflicting current application 09/911,409 recites "a first control circuit which controls writing or reading of the still-image data and (emphasis) the moving-image data..." and does not recite "a reception circuit". It would have been obvious to make the claimed limitations of the application "a reception circuit" are narrower than the claimed limitation of application 09/911,409.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. Claims 1-34 of this application conflict with claims 1-25 of Application No. 09/911,409. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

Claim Objections

7. Claims 1, 26, 31 and 32 are objected to because of the following informalities: MPU recited at line 5 of claim 1, MPU recited at line 3 of claims 26, 31, and 32. MPU should be read "microprocessor unit". Appropriate correction is required.

Response to Arguments

8. Applicant's arguments, see pages 9-12, filed 03/30/2005, with respect to the rejection(s)of claim(s) 1-34 under the statutory basis for the previous rejection have

been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art references.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 6, 21, 26, 28, 30, 32, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al (IDS cited, JP 09-281933) in view of Shimamoto (previously cited, US 6,147,672).

11. As to claim 1, Nitta et al teach at least a RAM(433)-incorporated driver (307) comprising (see drawing 3):

a. [recited in lines 4-7 of claim 1]

Still-frame picture data is transferred from the CPU 304 (drawing 1) to RAM 433 (see detail in drawing 3, drawing 3 is detailed of drawing 1) in a data driver 307 (drawing 3). It is obvious to provide the still-frame picture data through a pin connector of the data driver 307. Thus, the still-frame pin connector defined a first port as claimed.

Moving video picture data, which requires multi gradation display, is processed by a moving video picture driver 311 (drawing 1) and sent to the data driver 307 (drawing 3) through a panel 302 (drawing 1) (see front page, Solution, lines 1-6). It is obvious to provide the moving-frame picture data through another pin connector of the

data driver 307. Thus, the moving-frame pin connector defined a second port as claimed. Or the given command (synchronized bus signal 310, address bus signal 301, control bus signal 303) input from the CPU and the moving video picture driver 311.

Animation display data of every one line are transmitted to the data driver LSI 307 from the animation controller 311 through the data bus 302 at a serial (see paragraph [0087]). It would have been obvious to provide inherently a reception circuit and the different signal as claimed.

Accordingly, it would have been obvious to provide male pins connectors of the IC column driver 307 that defines inherently a first port and a second port. CPU 304 and the moving video picture driver 311 define an external MPU.

[recited in lines 10-11 of claim 1]

First, the writing of the indicative data (still image, see detail in [0070]) to a memory cell 433 is explained (paragraph [0072]).

Next, read-out (display action, moving picture, see detail in [0082]) of the indicative data from the memory cell 433 is explained (paragraph [0076]). The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data held at the memory cell 433 [0077]. The animation (moving picture) controller 311 performs FRC control (see detail in [0082]).

Therefore, a RAM 433 stores a still-image and a moving-image.

[recited in lines 12-14 of claim 1]

a column address decoder 429 and a row address decoder 425 (a first control circuit, drawing 3) controls writing/reading of the indicative data (a still image) on this memory cell 433 (see detail in paragraph [0059]).

[recited in lines 15-17 of claim 1]

CPU 304 (a second control circuit) carries out reading appearance of the indicative data in memory 305 and carries out it about a still picture, and this is written in the memory cell 433 of the data driver LSI 307 (see paragraph [0070]).

Therefore, the first control circuit and the second control circuit are controlled independently.

b. Accordingly, Nitta et al teach all of the claimed limitations of claim 1, except for "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see fig. 10, col. 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nitta's reception of driver 307 including differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

12. As to claim 6, Shimamoto teach the serial transfer line (serial interface 206, fig. 2) is a transfer line in accordance with an LVDS standard (col. 3, lines 60-61).

13. As to claim 21, Nitta et al disclose in drawing 1 showing the column driver 307 (a plurality of first electrodes) and the row driver 308 (a plurality of second electrodes) drive the display panel 309 (a panel).

14. As to claim 26, Nitta et al teach the microprocessor unit is defined by the CPU 304 (drawing 1) and the moving video picture driver 311 (front page, Solution, lines 4-5) which supply the command (synchronized bus signal 310, address bus signal 301, control bus signal 303), the still image data, and the moving image data to the display unit 309 (drawing 1).

15. As to claim 28, Nitta et al teach at least a RAM(433)-incorporated driver (307) (see drawing 3) comprising:

c. [recited in lines 4-7 of claim 28]

Still-frame picture data is transferred from the CPU 304 (drawing 1) to RAM 433 (see detail in drawing 3, drawing 3 is detailed of drawing 1) in a data driver 307 (drawing 3). It is obvious to provide the still-frame picture data through a pin connector of the data driver 307. Thus, the still-frame pin connector defined a first port as claimed.

Moving video picture data, which requires multi gradation display, is processed by a moving video picture driver 311 (drawing 1) and sent to the data driver 307 (drawing 3) through a panel 302 (drawing 1) (see front page, Solution, lines 1-6). It is obvious to provide the moving-frame picture data through another pin connector of the data driver 307. Thus, the moving-frame pin connector defined a second port as

claimed. Or the given command (synchronized bus signal 310, address bus signal 301, control bus signal 303) input from the CPU and the moving video picture driver 311.

Animation display data of every one line are transmitted to the data driver LSI 307 from the animation controller 311 through the data bus 302 at a serial (see paragraph [0087]). It would have been obvious to provide inherently a reception circuit and a different signal as claimed.

Accordingly, it would have been obvious to provide male pins connectors of the IC column driver 307 that defines inherently a first port and a second port. CPU 304 and the moving video picture driver 311 define the external MPU.

[recited in lines 10-11 of claim 28]

First, the writing of the indicative data (still image, see detail in [0070]) to a memory cell 433 is explained (paragraph [0072]).

Next, read-out (display action, moving picture, see detail in [0082]) of the indicative data from the memory cell 433 is explained (paragraph [0076]). The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data held at the memory cell 433 [0077]. The animation controller 311 performs FRC control (see detail in [0082]).

Therefore, a RAM 433 stores a still-image and a moving-image.

[recited in lines 12-14 of claim 28]

a column address decoder 429 and a row address decoder 425 (a first control circuit, drawing 3) controls writing/reading of the indicative data (a still image) on this memory cell 433 (see detail in paragraph [0059]).

Read-out (display action) of the indicative data from a memory cell 433 is explained (paragraph [0076]). The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data held at the memory cell 433 (paragraph [0077]). The animation (moving picture) controller 311 performs FRC control (paragraph [0082], one last line).

Therefore, teaching of Nitta et al meet the claimed limitation "a first control circuit which controls writing or reading of the still-image data and (emphasis) the moving-image data that has been input separately through the first port or the second port, with respect to the RAM."

[recited in lines 15-17 of claim 28]

CPU 304 (a second control circuit) carries out reading appearance of the indicative data in memory 305 and carries out it about a still picture, and this is written in the memory cell 433 of the data driver LSI 307 (see paragraph [0070]).

Therefore, the first control circuit and the second control circuit are controlled independently.

d. Accordingly, Nitta et al teach all of the claimed limitations of claim 1, except for "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see fig. 10, col. 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nitta's reception of driver 307 including differentially

amplifies the differential signal input from the second port and creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

16. As to claim 30, Nitta et al disclose in drawing 1 showing the column driver 307 (a plurality of first electrodes) and the row driver 308 (a plurality of second electrodes) drive the display panel 309 (a panel).

17. As to claim 32, Nitta et al teach the microprocessor unit is defined by the CPU 304 (drawing 1) and the moving video picture driver 311 (front page, Solution, lines 4-5) which supply the command (synchronized bus signal 310, address bus signal 301, control bus signal 303), the still image data, and the moving image data to the display unit 309 (drawing 1).

18. As to claim 34, Nitta et al teach the first pin connector and the second pin connector are connected inherently in parallel of the driver 307.

19. Claims 27, 29, 31 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al in view of Shimamoto, and further in view of Kida et al (previously cited),

20. As to claim 27, Nitta et al teach at least a RAM(433)-incorporated driver (307) (see drawing 3) comprising:

e. [recited in lines 4-7 of claim 28]

Still-frame picture data is transferred from the CPU 304 (drawing 1) to RAM 433 (see detail in drawing 3, drawing 3 is detailed of drawing 1) in a data driver 307 (drawing 3). It is obvious to provide the still-frame picture data through a pin connector of the data driver 307. Thus, the still-frame pin connector defined a first port as claimed.

Moving video picture data, which requires multi gradation display, is processed by a moving video picture driver 311 (drawing 1) and sent to the data driver 307 (drawing 3) through a panel 302 (drawing 1) (see front page, Solution, lines 1-6). It is obvious to provide the moving-frame picture data through another pin connector of the data driver 307. Thus, the moving-frame pin connector defined a second port as claimed. Or the given command (synchronized bus signal 310, address bus signal 301, control bus signal 303) input from the CPU and the moving video picture driver 311.

Animation display data of every one line are transmitted to the data driver LSI 307 from the animation controller 311 through the data bus 302 at a serial (see paragraph [0087]). It would have been obvious to provide inherently a reception circuit and a different signal as claimed.

Accordingly, it would have been obvious to provide male pins connectors of the IC column driver 307 that defines inherently a first port and a second port. CPU 304 and the moving video picture driver 311 define the external MPU.

[recited in lines 10-11 of claim 28]

First, the writing of the indicative data (still image, see detail in [0070]) to a memory cell 433 is explained (paragraph [0072]).

Next, read-out (display action, moving picture, see detail in [0082]) of the indicative data from the memory cell 433 is explained (paragraph [0076]). The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data held at the memory cell 433 [0077]. The animation controller 311 performs FRC control (see detail in [0082]).

Therefore, a RAM 433 stores a still-image and a moving-image.

[recited in lines 12-14 of claim 28]

a column address decoder 429 and a row address decoder 425 (a first control circuit, drawing 3) controls writing/reading of the indicative data (a still image) on this memory cell 433 (see detail in paragraph [0059]).

Read-out (display action) of the indicative data from a memory cell 433 is explained (paragraph [0076]). The FRC selector 435 changes into the 1-bit FRC data 436 the indicative data held at the memory cell 433 (paragraph [0077]). The animation (moving picture) controller 311 performs FRC control (paragraph [0082], one last line).

Therefore, teaching of Nitta et al meets the claimed limitation "a first control circuit which controls writing or reading of the still-image data and (emphasis) the moving-image data that has been input separately through the first port or the second port, with respect to the RAM."

[recited in lines 15-17 of claim 28]

CPU 304 (a second control circuit) carries out reading appearance of the indicative data in memory 305 and carries out it about a still picture, and this is written in the memory cell 433 of the data driver LSI 307 (see paragraph [0070]).

Therefore, the first control circuit and the second control circuit are controlled independently.

f. Accordingly, Nitta et al teach all of the claimed limitations of claim 1, except for "a reception circuit which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state."

However, Shimamoto teaches a LCD panel comprising a reception circuit (103) which differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state (see fig. 10, col. 8, lines 58-67).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nitta's reception of driver 307 including differentially amplifies the differential signal input from the second port and creates the moving image data in a parallel state, in view of the teaching of Shimamoto's reference because this would prevent an influence of electric wave radiation on the ambience, improve a high resolution display mode, and reduce the number of interface signal lines as taught by Shimamoto (col. 2, lines 36-41).

Accordingly, the combination of Nitta et al with Shimamoto teach all of the claimed limitation of claim 27, except for "wherein the still-image data can be rewritten irrespective of the timing at which the moving-image data is rewritten in the RAM."

However, Kida et al teach a related memory driving display comprising:

The memory control means rewrites the pixel data in a predetermined storage area among the plurality of storage areas in the first and second memories (col. 3, lines 18-20).

The first mixture displaying period starts at time t3, and in the field memory 34B, the number of pixels in the horizontal direction in the pixel data B2 of one field is reduced in accordance with the address in the storage area SA2 for a motion image by the memory control circuit and the reduced pixel data is written into only the storage area SA2 for a motion image by the write enable signal WR2 (refer to FIG. 14, col. 16, lines 43-50).

In this case, the pixel data in the storage area SA1 in the memory 34B which is not rewritten coincides (irrespective of the timing) with the pixel data which has already been written in the storage area SA1 in the memory 34A (col. 16, lines 51-54).

The second mixture displaying period starts at time t4 when the writing of the pixel data to the field memory 34B ends (col. 16, lines 55-57).

Thus, the time t3 and the time 4 are irrespective of the timing as claimed.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the Nitta's RAM including the still-image data can be rewritten irrespective of the timing at which the moving-image data is rewritten in the RAM, in view of the teaching in the Kido et al's reference, because this would provide sizes of the display areas of the motion image and the still image can be set to arbitrary sizes as taught by Kido et al (see col. 18, lines 26-28), and see col. 18, lines 29-33 for more motivation.

21. As to claim 29, Nitta et al disclose in drawing 1 showing the column driver 307 (a plurality of first electrodes) and the row driver 308 (a plurality of second electrodes) drive the display panel 309 (a panel).

22. As to claim 31, Nitta et al teach the microprocessor unit is defined by the CPU 304 (drawing 1) and the moving video picture driver 311 (front page, Solution, lines 4-5) which supply the command (synchronized bus signal 310, address bus signal 301, control bus signal 303), the still image data, and the moving image data to the display unit 309 (drawing 1).

23. As to claim 33, Nitta et al teach the first pin connector and the second pin connector are connected inherently in parallel of the driver 307.

24. Claims 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al in view of Shimamoto, and further in view of Silverman et al (previously cited, US 6,370,603).

As to claims 11 and 16, Nitta et al and Shimamoto teach all of the claimed limitations of claim 1, except for the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard.

However, Silverman et al teach the serial transfer line is a transfer line (serial interface engine 206, fig. 2) in accordance with a USB standard and an IEEE 1394 standard (column 8, lines 19-23).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nitta's reception of driver 307 including the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard, in view of the teaching of Silverman's reference because this would provide an improved technique for effecting digital communications between digital devices and

system using different communication protocols as taught by Silverman (column 4, lines 10-13).

25. Claims 2-5, 7-10 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al in view of Shimamoto, and further in view of Chida (previously cited, US 6,313,863).

As to claim 2, the combination of Nitta et al with Shimamoto teach all of the claimed limitations of claim 1, except for a data validation signal generation circuit.

However, Chida teaches a halt control circuit (a system control unit 26, fig. 1). A validity table 26-1 manages validities of each image block designated by a validity designating unit 36. A special coded data table 26-2 manages a special coded image. A static image table 26-3 manages a static image. A validity designating unit 34 designates validities of each block of an image in accordance with instructions from the system control unit 26 that controls a control unit 34 based on the validity table 26-1(fig. 1, col. 4, lines 23-30).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Shimamoto's reception circuit including a data validation signal generation circuit, in view of the teaching of Chida's reference because this would improve the quality of an image that is transmitted through a communication channel or line, and improve a quality image in an acceptable amount of time from a partner's terminal as taught by Chida (col. 2, lines 40-45).

26. As to claims 3-5, Chida teaches when the receiving side displays only the valid area, the system control unit 26 of the receiving side controls the synthesizing/

processing unit 125 so that unit 125 extracts a part of the image stored in the receiving video RAM 121 based on the validity information of the blocks (fig. 11a, col. 9, lines 48-52).

27. As to claims 7-10, Shimamoto teaches the serial transfer line is a transfer line in accordance with an LVDS standard (col. 3, lines 60-61).

28. As to claims 22-25, Nitta et al disclose in drawing 1 showing the column driver 307 (a plurality of first electrodes) and the row driver 308 (a plurality of second electrodes) drive the display panel 309 (a panel).

29. Claims 12-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta et al in view of Shimamoto, and further in view of Silverman et al.

As to claims 12-20, the combination of Nitta et al with Shimamoto teach all of the claimed limitations of claim 1, except for the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard.

However, Silverman et al teach the serial transfer line (serial interface engine 206, fig. 2) is a transfer line in accordance with a USB standard and an IEEE 1394 standard (column 8, lines 19-23).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Nitta's reception of driver 307 including the serial transfer line is a transfer line in accordance with a USB standard and an IEEE 1394 standard, in view of the teaching of Silverman's reference because this would provide an improved technique for effecting digital communications between digital devices and

system using different communication protocols as taught by Silverman et al (column 4, lines 10-13).

Response to Arguments

30. Applicant's arguments with respect to claims 1-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Nguyen whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick N. Edouard can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen
Patent Examiner
Art Unit 2674

KMN
April 28, 2005

XIAO WU
PRIMARY EXAMINER